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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,393	11/21/2003	Alexei V. Galatenko	03-0937/L13.12-0257	2571

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EXAMINER	
DOAN, NGHIA M	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 05/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/719,393	GALATENKO ET AL.
	Examiner	Art Unit
	Nghia M. Doan	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/21/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application filed on 11/21/2003, claims 1-20 are pending.

Drawings

2. The drawings are objected to because **figure 2, element 108 is not contact to detail, figure 3, elements 208, 218, and 220 are not contact to details and element 204 goes cross the boundary of detail** . Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3,5,6, 11-13, 15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Andreev et al. (US 2005/0091625).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

5. **With respect to claim 1**, Andreev et al. disclose a process of positioning megacells that are included in an initial integrated circuit layout that violates design rules, the circuit layout having sides defining sides of a chip (pg.1, ¶ 14, ll. 1-3), the process comprising steps of:

inflating a size of at least some of the megacells (pg.1, ¶ 12, ll. 3-7; ¶ 16, ll. 1-4);

placing the megacells in a footprint of the circuit to reduce placement complexity (Fig. 1, pg.2, ¶ 21, ll. 1-6); and

permuting megacell placements to reduce placement complexity (Fig. 1, Step 30, pg.3, ¶ 44, ll. 1-4).

6. **With respect to claim 2**, Andreev et al. disclose the process claim 2, wherein step of inflating size of megacells (fig 4, step 70) comprises, each megacell of a first type:

identifying distance between an edge the megacell and each side the chip (Fig. 4, steps 70-86; Fig3, steps 60-62; pg.2, ¶ 29, ll. 5-10),

identifying distance between center of the megacell and center of another megacell of the first type (Fig. 1, step 14; pg.2, ¶ 21, ll. 1-6; pg. 3, ¶ 35-37; and ¶ 43, ll. 2-4), and

applying an inflation factor to the sides of the megacell (Fig. 1, step 18-32; pg.1, ¶ 16, ll. 1-3; ¶ 43, ll. 2-4).

7. **With respect to claim 3**, Andreev et al. disclose the process of claim 2, wherein the inflation factor is calculated by:

identifying a number of pins in each half of the megacell in each of two orthogonal directions (Fig. 3, step 50, pg.2, ¶ 22), and

for each direction, at least in part basing the inflation factor for sides of the megacell in the respective direction on the number of pins in both halves of the megacell (Fig. 3, step 50, pg.2, ¶ 22; pg3, ¶ 31, ll. 1-4).

8. **With respect to claim 5**, Andreev et al. disclose the process of claim 1, wherein the placement of the megacells comprises:

placing all fixed megacells and blockages in the footprint (pg. 2, ¶ 21, ll. 1-6),

generating a list of free rectangles in the footprint that do not contain megacells and blockages (Fig. 4, pg. 3, ¶ 28, ll. 1-5; pg. 3, ¶ 31, ll. 1-4),

for each not-fixed megacell starting with a not- fixed megacell selected on the basis of size (pg. 2, ¶ 24, ll. 5-6), placing the megacell in a free rectangle that is large enough to receive the megacell (pg. 3, ¶ 41, ll. 1-4), and

applying a transformation movement to the megacell if the movement reduces placement complexity (fig. 1, step 30; pg. 3, ¶ 40 ll. 1-5; claim 13).

9. **With respect to claim 6**, Andreev et al. disclose the process of claim 5, wherein the transformation movement is selected from the group consisting of shifting, rotating and flipping (fig. 1, step 30; pg. 3, ¶ 40 ll. 1-5).

10. **With respect to claim 11**, Andreev et al. disclose a computer usable medium having a computer readable program embodied therein for addressing data to position megacells that are included in an initial integrated circuit layout that violates design rules, the circuit layout having sides defining sides of a chip (pg. 1, ¶ 10, ll. 1-3), the computer readable program comprising:

computer readable code for causing the computer to inflate a size of at least some of the megacells (pg.1, ¶ 12, ll. 3-7; ¶ 16, ll. 1-4; pg. 4, claim 12, ll. 5-7);

computer readable code for causing the computer to place the megacells in a footprint of the circuit to reduce placement complexity (Fig. 1, pg.2, ¶ 21, ll. 1-6; pg. 4, claim 12, ll. 11-14); and

computer readable code for causing the computer to permute megacell placements to reduce placement complexity (Fig. 1, Step 30, pg.3, ¶ 44, ll. 1-4; claim 13, ll. 8-10).

11. **With respect to claim 12**, Andreev et al. disclose the computer usable medium of claim 11, wherein the computer readable code that causes the computer to inflate sizes of megacells (fig 4, step 70) comprises:

computer readable code for causing the computer to identify a distance between an edge on each megacell of a first type and each side of the chip (Fig. 4, steps 70-86; Fig3, steps 60-62; pg.2, ¶ 29, ll. 5-10; claim 1, ll. 8-9; claim 16, ll. 4-9),

computer readable code for causing the computer to identify a distance between a center of the megacell and a center of another megacell of the first type (Fig. 1, step 14; pg.2, ¶ 21, ll. 1-6; pg. 3, ¶ 35-37; and ¶ 43, ll. 2-4), and

computer readable code for causing the computer to apply an inflation factor to the sides of the megacell (Fig. 1, step 18-32; pg.1, ¶ 16, ll. 1-3; ¶ 43, ll. 2-4; claim 17).

12. **With respect to claim 13**, Andreev et al. disclose the computer usable medium of claim 12, wherein the computer readable program further includes:

computer readable code for causing the computer to identify a number of pins in each half of the megacell in each of two orthogonal directions (Fig. 3, step 50, pg.2, ¶ 22; claim 16), and

computer readable code for causing the computer to calculate the inflation factor for a side of the megacell along one of the directions based at least in part on the number of pins in both respective halves of the megacell (Fig. 3, step 50, pg.2, ¶ 22; pg3, ¶ 31, ll. 1-4, claim 17).

13. **With respect to claim 15**, Andreev et al. disclose the computer usable medium of claim 11, wherein the computer readable code for causing the computer to place the megacells comprises:

computer readable code for causing the computer to place all fixed megacells and blockages in the footprint (pg. 2, ¶ 21, ll. 1-6; claim 14),

computer readable code for causing the computer to generate a list of free rectangles in the footprint that do not contain megacells and blockages (Fig. 4, pg. 3, ¶ 28, ll. 1-5; pg. 3, ¶ 31, ll. 1-4; claim 15),

computer readable code for causing the computer to place each not-fixed megacell in a free rectangle (pg. 2, ¶ 24, ll. 5-6) that is large enough to receive the megacell (pg. 3, ¶ 41, ll. 1-4, claim 17), and

computer readable code for causing the computer to apply a transformation movement to the megacell if the movement reduces placement complexity (fig. 1, step 30; pg. 3, ¶ 40 ll. 1-5, claim13).

14. **With respect to claim 16**, Andreev et al. disclose the process of claim 15, wherein the transformation movement is selected from the group consisting of shifting, rotating and flipping (fig. 1, step 30; pg. 3, ¶ 40 ll. 1-5).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hossain et al. (US 6,014,506) and further in view of Applicant's Admitted Prior Art (AAPA).

17. **With respect to claims 1 and 11,** Hossain et al. disclose a process of positioning megacells that are included in an initial integrated circuit layout that violates design rules, the circuit layout having sides defining sides of a chip (col. 6, ll. 10-20), the process performs associated with a computer usable medium having a computer readable program (col. 4, ll. 51-60; fig. 2, elements HDL, 32, and 34; col. 5, ll. 3-15) comprising steps of:

inflating a size of at least some of the megacells (col.6, ll. 32-37 and ll. 60-67; claim 1, step 2);

placing the megacells in a footprint of the circuit to reduce placement complexity (claim 1, ll. 32-34, and step 3); and

permuting megacell placements to reduce placement complexity (claim 1, steps 3-6).

18. Hossain et al. do not explicitly disclose the term "megacell". However, Hossain et al. disclose the used of cells or modules (col.1, ll. 11-15) and bigger cells (col.2, ll. 40-43)

19. AAPA teaches that the "megacells" occupy a large area (AAPA, Background of the invention, pg. 1, ll. 14-15)

20. Therefore, it would have been obvious to one of person ordinary skill in the art would recognized that the megacells mentioned in AAPA is the same as the cells of the integrated circuit teaching in Hossain et al., because both the megacell and the bigger cell could also require the used of a large area.

21. **With respect to claims 2 and 12**, Hossain et al. disclose the process claim 1 and claim 11, respectively, wherein step of inflating size of megacells (fig 6, col.8, ll. 51-63) comprises, each megacell of a first type:

identifying distance between an edge the megacell and each side the chip (Fig. 6, col. 6, ll. 63-67),

identifying distance between center of the megacell and center of another megacell of the first type (col. 6, ll. 39-49), and

applying an inflation factor to the sides of the megacell (col. 6, ll. 39-49, col. 8, ll. 17-22).

22. **With respect to claims 3 and 13**, Hossain disclose et al. the process of claim 2 and claim 12, respectively, wherein the inflation factor is calculated by:

identifying a number of pins in each half of the megacell in each of two orthogonal directions (col. 6, ll. 39-49), and

for each direction, at least in part basing the inflation factor for sides of the megacell in the respective direction on the number of pins in both halves of the megacell (col. 6, ll. 39-49, col. 7, ll. 29-59).

23. **With respect to claims 4 and 14**, Hossain et al. disclose the process of claim 2 and claim 12, respectively, wherein the megacell has dimensions of m x n, and the inflation factor in the m dimension is calculated based on ldyn * (npleft + npright) and the inflation factor in the n dimension is calculated based on ldyn * (npupper + npzower), where ldyn is an inflation coefficient, npleft and npright are a number of pins in respective halves of the megacell divided along the m dimension, and npupper and npzower are a number of pins in respective halves of the megacell divided along the n dimension (col. 6, ll. 39-49).

24. **With respect to claims 5 and 15**, Hossain et al. disclose the process of claim 1 and claim 11, respectively, wherein the placement of the megacells comprises:

placing all fixed megacells and blockages in the footprint (col.3, ll. 28-30),

generating a list of free rectangles in the footprint that do not contain megacells and blockages (col. 8, ll. 55-63),

for each not-fixed megacell starting with a not- fixed megacell selected on the basis of size, placing the megacell in a free rectangle that is large enough to receive the megacell (col. 8, ll. 51-67), and

applying a transformation movement to the megacell if the movement reduces placement complexity (col.8 , ll. 23-27 and ll. 36-38).

25. **With respect to claims 6 and 16**, Hossain et al. disclose the process of claim 5 and claim 15, respectively, wherein the transformation movement is selected from the group (col. 9, ll. 19-21) consisting of shifting, rotating and flipping (fig. 7, col. 8, ll. 25-27, ll. 36-38; ll. 66-67, col. 9, ll. 1-5).

26. **With respect to claims 7 and 17**, Hossain et al. disclose the process claim 5 and claim 15, respectively, wherein the step placing not-fixed megacells starts with the largest megacell not-fixed (col. 2, ll. 40-46).

27. **With respect to claims 8 and 18**, Hossain et al. disclose the process of claim 1 and claim 11, respectively, wherein the permutation of megacell placements comprises:

swapping positions of megacells of each pair of not-fixed megacells if the swapping reduces placement complexity (col. 8, ll. 17-23), and

applying a transformation movement to each megacell if the movement reduces placement complexity (fig. 7, col. 8, ll. 25-27, ll. 36-38; ll. 66-67, col. 9, ll. 1-5) .

28. **With respect to claims 9 and 19**, Hossain et al. disclose the process of claim 8 and claim 18, respectively, wherein the transformation movement selected the group (col. 9, ll. 19-21) consisting of shifting, rotating and flipping (fig. 7, col. 8, ll. 25-27, ll. 36-38; ll. 66-67, col. 9, ll. 1-5).

29. **With respect to claims 10 and 20**, Andreev et al. disclose the process of claim 8 and claim 18, respectively, wherein the swapping and application of transformation movement is iteratively performed (col. 3, ll. 60-64).

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References Gasanov et al. (US 6,637,016), Heng et al. (US 6,189,132) and Cohn et al. (US 5,535,134) teach method of arrange or modifying a circuit layout based on different characteristics and constraint functional, such as: design rules, timing constraint, or area criteria requirements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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